

**REMARKS**

This responds to the Office Action mailed on January 25, 2007, and the Advisory Action mailed April 2, 2007.

Claims 1, 8, 12 and 17 are amended, no claims are canceled herein, and no claims are added; as a result, claims 1, 3-8 and 11-18 are now pending in this application.

***§112 Rejection of the Claims***

The rejection of claims 1, 3-8 and 11-18 under 35 U.S.C. § 112, first paragraph, has been maintained. Specifically, the Office Action states that claims 1, 3-8 and 11-18 are rejected because of the lack of support of the written description for the following limitations: (1) “a processor cache and a translation look-aside buffer (TLB)”; (2) “the RTT has capacity to store all physical page numbers associated with the processing node”; and (3) “wherein each TLB translates memory references from its associated processor to the shared memory within the processing node.”

Applicant respectfully draws the Examiner’s attention to the amendments in the Specification and in the Drawings made in the previous Response mailed March 22, 2007. In addition, claims 1, 8, 12 and 17 have been amended to more clearly define Applicant’s claimed invention as requested by the Examiner. Applicant respectfully submits that the limitations in amended claims 1, 8, 12 and 17 are fully supported from Applicant’s Specification as amended in the previous Response.

First of all, as noted at Fig. 9 (920 and 940), p. 2, lines 15-16 and lines 4-6 of the third paragraphs from the original paragraph beginning at page 6, line 19 (see the previous Office Action, p. 3, lines 23-25), Applicant clearly teaches using a processor having “a processor cache and a translation look-aside buffer (TLB).”

Secondly, as noted at p. 6, lines 28-29, Applicant clearly teaches that “the RTT [on the remote node] contains translation information for an entire virtual memory address space associated with the remote node.” It is inherent from the teaching that the RTT on the remote node has capacity to store all physical page numbers associated with the remote node (i.e.,

processing node). In addition, claims 1, 8, 12 and 17 have been amended to more clearly define this feature as requested by the Examiner.

Finally, as noted at Fig. 12 (402, 404, 406) and lines 6-10 of the fourth paragraph from the original paragraph beginning at p 6, line 19 (see the previous Office Action, p. 4, lines 12-16), Applicant teaches that “a virtual address is translated into a physical address locally using a Translation Look-Aside Buffer (TLB)” if the Vnode field of the virtual address is the same as the local node. Claims 1, 8, 12 and 17 have been amended to more clearly define Applicant’s invention as requested by the Examiner.

For these reasons, the limitations above are fully supported by Applicant’s Specification as amended in the previous Response mailed March 22, 2007. Reconsideration is respectfully requested.

#### §103 Rejection of the Claims

Claims 1, 3, 5-8 and 11-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Scott et al. (US 6,925,547; hereinafter ‘Scott’) in view of Fossum et al. (US 4,888,679; hereinafter ‘Fossum’).

As noted in the discussion of §112 rejection, claims 1, 8, 12 and 17 have been amended to more clearly define Applicant’s claimed invention. Applicant respectfully submits that neither Scott nor Fossum, alone or in combination, teach or suggest a multiprocessor computer system as taught by Applicant and claimed in amended claims 1, 8, 12 and 17.

Applicant’s computer system employs remote translation. Under Applicant’s remote translation, as noted at Fig. 12 and the third and the fourth paragraphs from the original paragraph beginning p. 6, line 19, a processor’s virtual address reference to its shared memory on the local node (i.e., “if the virtual node is the same, or equal to, the local node”) is translated locally using a Translation Look-Aside Buffer (TLB) on the local node. In contrast, the processor’s virtual address reference to local memory on a remote node (i.e., “if the virtual node is not the same as the local node”) is sent to the remote node and translated remotely using a Remote Translation Table (RTT) on the remote node. See the previous Office Action, p. 3, line 20 through p. 4, line 20. The TLB and the RTT are entities separate from each other. Claims 1, 8, 12 and 17 have been amended to more clearly defined Applicant’s claimed invention.

Scott describes a method for performing remote address translation in a multiprocessor system (Abstract, lines 1-2). Specifically, Scott describes an address translation method where a virtual address for a remote node is sent to the remote node and translated into a physical address at the remote node using a translation look-aside buffer (TLB) (id. lines 2-19).

Fossum describes a method and apparatus using a cache and main memory for both vector processing and scalar processing units (Abstract). Specifically, Fossum describes a scalar processor sending a vector load command to a vector processor, and also sending a vector prefetch request to the cache in response to a vector load instruction (col. 3, lines 17-20).

Neither Scott nor Fossum, however, alone or in combination, teach or suggest using a TLB to translate memory requests from a local node while using a RTT to translate memory requests from a remote node as taught by Applicant and claimed in amended claims 1, 8, 12 and 17.

First of all, the Office Action states that:

(Office Action, p. 4, lines 12-17) From the description [page 6, lines 19-30 and page 7, lines 1-8 of Applicant's Specification], it appears that the [Applicant's] address transaction scheme would use the local translation means (i.e., the RTT located at the local processor/node) to translate the address if the virtual address corresponds to a local address space, and would use the remote translation means (i.e., the RTT located at the remote processor/node) to translate the address if the virtual address corresponds to a remote address space.

The Office Action also states that col. 17, lines 35-45, col. 2, lines 65-67, and col. 3, lines 1-23 of Scott shows using the same RTT to translate memory requests not only from a remote node but also from a local node (Office Action, p. 5, lines 1-10). Based on this, the Office Action further states that there is no difference between Applicant's translation scheme and Scott's approach. Id.

As noted in the discussion of rejections under § 112 above, however, Applicant clearly teaches and claims using the TLB to translate memory references from a local processing node while using the RTT to translate memory references from another (i.e., remote) processing node. Unlike the assertion in the Office Action, Applicant's RTT is used to translate virtual address references to a local node when that memory reference is coming from a remote node. A TLB associated with a local processor exists separate from the RTT and is used to translate virtual

address references to the local node by the local processor. Under Applicant's claimed invention, therefore, accesses from remote nodes do not have to fight local processes for space in the TLB. This reduces churning in the TLB.

In contrast to Applicant's separate translation approach for local and remote references, under Scott's approach, the TLB in a system HUB (SHUB) is used for both local and remote address references. Scott states that:

(col. 14, lines 9-13) If the connection endpoint is the **local node**, then the address translation uses a [external] TLB on the local SHUB. However, if the connection endpoint is a remote node, the address translation uses a [external] TLB on the remote node.

(col. 14, lines 47-52) The address translation mechanism used by CE 64 uses an external TLB located on the local SHUB, or an external TLB located on a remote SHUB, but **does not use the TLBs which are used by the processors themselves to perform translation**. Thus, the TLBs used by CE 64 may be referred to as "external" TLBs since they are external to the processors.

(col. 18, line 65 through col. 19, line 4) Thus, the address translation mechanism may be used to perform both local and remote address translations, with the [external] TLB on the local SHUB used for translating a virtual address if a CD indicates that the **local node** is the connection endpoint, and the [external] TLB on a remote SHUB used for translating the virtual address if a CD indicates that the remote node is the endpoint.

Although Scott discloses that the processor's TLB is separate from the [external] TLB in the SHUB, the TLBs associated with the processors do not participate in translating memory references to the local node by the processors. Instead, as quoted above and admitted in the Office Action (p. 5, lines 4-8), the separate [external] TLB in the local SHUB translates memory references by the local processors to the local node as well as memory references to the local node received from other remote nodes. This is a different approach from Applicant's invention claimed in amended claims 1, 8, 12 and 17.

For the reasons discussed above, neither Scott nor Fossum, alone or in combination, teach or suggest a multiprocessor computer system having latency tolerant and yet scalable shared memory as taught by Applicant and claimed in amended claims 1, 8, 12 and 17. Reconsideration is respectfully requested.

With regard to claims 3, 11, 13 and 18, claims 3, 11, 13 and 18 are patentable as depending on a patentable base claim. In addition, neither Scott nor Fossum, alone or in combination, teach or suggest the shared memory having a plurality of cache coherence directories as taught by Applicant and claimed in claims 3, 11, 13 and 18.

The Office Action states that Scott discloses the same limitation (p. 7, lines 9-15). As support of this, the Office Action points to col. 5, lines 47-67 of Scott, which partly states:

...In one embodiments, all of the coherence information is passed across the bus in the form of messages, and each processor on the bus “snoops” by monitoring the addresses on the bus and, if it finds the address of data within its own cache, invalidating that cache entry. Other cache coherence schemes can be used as well...

Applicant respectfully disagrees. Although the cited portion discloses use of a cache coherence method, the portion does not teach or suggest the specific way of **using cache coherence directories located in the shared memory** to maintain cache coherence as described and claimed by Applicant. Applicant is unable to find such a teaching in any of the references considered in the Office Action. Reconsideration is respectfully requested.

With regard to claims 6 and 15, claims 6 and 15 are patentable as being dependent on a patentable base claim. In addition, neither Scott nor Fossum, alone or in combination, teach or suggest using a scalar processing unit having a scalar cache memory with a subset of cache lines stored in a processor cache as taught by Applicant and claimed in claims 6 and 15.

The Office Action (p. 7, line 20 through p. 8, line 2) states that Fossum teaches the same limitation. As support of this, the Office Action points to Fig. 1 (CACHE 24) and col. 4, lines 15-54 of Fossum.

Applicant respectfully disagrees. Although the cited portions show use of a cache associated with both a scalar processor (21) and a vector processor (22), the portions do not show using an additional cache dedicated to the scalar processor as taught by Applicant and claimed in claims 6 and 15. Furthermore, Fossum does not teach or suggest the specific way of connecting the scalar cache memory (920) to the cache (120) by having the scalar cache memory (920) contain a subset of cache lines stored in the cache (120) as taught by Applicant and claimed in claims 6 and 15. Applicant is unable to find such a teaching in any of the references considered in the Office Action. Reconsideration is respectfully requested.

**AMENDMENT AND RESPONSE UNDER 37 CFR § 1.116 – EXPEDITED PROCEDURE**

Serial Number: 10/643,585

Filing Date: August 18, 2003

Title: LATENCY TOLERANT DISTRIBUTED SHARED MEMORY MULTIPROCESSOR COMPUTER

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Claim 4, 5, 7, 14 and 16 are patentable as being dependent on a patentable base claim.

**CONCLUSION**

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

**Reservation of Rights**

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of

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priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

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Date April 23, 2007

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**CERTIFICATE UNDER 37 CFR 1.8:** The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22343-1450 on this 23 day of April 2007.

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